Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – SUMMER 2021

Subject Code:3140707 Date:06/09/2021

Subject Name:Computer Organization & Architecture

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	State differences between hardwired control unit and microprogrammed control unit.	**03**
	(b)	Explain register stack and memory stack.	**04**
	(c)	Show the contents of registers E, AC, BR, QR and SC during the process of multiplying 11111 with 10101.	**07**
Q.2	**(a)**	Write down RTL statements for the fetch and decode operation of basic computer.	**03**
	(b)	Define pipelining. For arithmetic operation (Ai *Bi + Ci) with a stream of seven numbers (i=1 to 7). Specify a pipeline configuration to carry out this task.	**04**
	(c)	Write a program to evaluate the arithmetic statement: A*B+C*D+E i. Using an accumulator type computer. ii. Using a stack organized computer.	**07**
		OR	
	(c)	A non-pipeline system takes to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?	**07**
Q.3	**(a)**	List down six major characteristics of RISC processors.	**03**
	(b)	Explain how (r-1)'s complement is calculated. Calculate 9's complement of 546700.	**04**
	(c)	Elaborate CPU-IOP communication.	**07**
		OR	
Q.3	**(a)**	List and explain major instruction pipeline conflicts.	**03**
	(b)	Define RTL. Give block diagram and timing diagram of transfer of R1 to R2 when P=1.	**04**
	(c)	Elaborate content addressable memory (CAM).	**07**
Q.4	**(a)**	Explain memory hierarchy in brief.	**03**
	(b)	Draw and explain flowchart for first pass of assembler.	**04**
	(c)	Explain using a flowchart how address of control memory is selected in microprogrammed control unit.	**07**
		OR	
Q.4	**(a)**	Briefly explain DMA.	**03**
	(b)	Write assembly level program to subtract two given numbers.	**04**
	(c)	Write the symbolic microprogram routine for the BSA instruction. Use the microinstruction format of basic microprogrammed control unit.	**07**

Q.5	**(a)**	How many AND gates and Adders will be required to multiply a 5 bit number with a 3 bit number? Also say size of adder (bits). How many bits will be there in the result?	**03**
	(b)	What do you mean by cache memory? Justify the need of cache memory in computer systems.	**04**
	(c)	Discuss multistage switching network with neat diagrams.	**07**

OR

Q.5	**(a)**	Explain the non-restoring methods for dividing two numbers.	**03**
	(b)	Discuss source-initiated transfer using handshaking in asynchronous data transfer.	**04**
	(c)	Elaborate cache coherence problem with its solutions.	**07**

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