Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2020

Subject Code:3130907 Date:04/03/2021

Subject Name:Analog & Digital Electronics

Time:10:30 AM TO 12:30 PM Total Marks:56

Instructions:

1. **Attempt any FOUR questions out of EIGHT questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Define Slew Rate, CMRR, & Input Offset Voltage.	**03**
	(b)	Compare inverting and non-inverting op-amps.	**04**
	(c)	Draw & explain in detail the logic diagram & the truth table of clocked SR flip-flop.	**07**
Q.2	**(a)**	Draw block diagram of an op-amp.	**03**
	(b)	Draw and explain working of zero crossing detector.	**04**
	(c)	List out and discuss all the ideal characteristics of an op-amp.	**07**
Q.3	**(a)**	For an inverting amplifier, $V_1 = 1V$, $V_2 = 3V$, $V_3 = 2V$ with $R_1 = R_2 = R_3 = 2K\Omega$ and $R_F = 3K\Omega$. Determine the output voltage.	**03**
	(b)	Design an R-C phase shift oscillator to produce a sinusoidal output at 1KHz, using capacitor value 0.01 μF.	**04**
	(c)	Write a short note on instrumentation amplifier using op-amp.	**07**
Q.4	**(a)**	Explain the application of an op-amp as an integrator.	**03**
	(b)	Design full adder logic circuit using 3 x 8 decoder and OR gates.	**04**
	(c)	Explain the circuit diagram of op-amp as a Peak detector.	**07**
Q.5	**(a)**	Design D FF using SR FF. Write truth table of D FF.	**03**
	(b)	Minimize following Boolean function using K-map: $F(A,B,C,D) = \Pi\, M(1, 2, 3, 8, 9, 11, 14) \bullet d(7, 15)$	**04**
	(c)	Given a logic function: Z = ABC + BC'D + A'BC. a) Make a truth table. b) Simplify using K-map. c) Realize simplified function using NAND gates only.	**07**
Q.6	**(a)**	Minimize following Boolean function using K-map: $Y(A,B,C,D) = \Sigma\, m(0, 3, 5, 6, 9, 10, 12, 15)$	**03**
	(b)	Implement the following logic function using 8:1 multiplexer: $F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$	**04**
	(c)	Design a 4-bit synchronous down counter using T flip-flops.	**07**
Q.7	**(a)**	Compare combinational logic circuit with sequential logic circuit.	**03**
	(b)	Draw basic internal structure of 7490 ripple counter IC. Design BCD counter using 7490 IC.	**04**
	(c)	Draw & explain R-2R ladder D/A converter with necessary equations.	**07**

Q.8	**(a)**	Draw the logic diagram of 4-bit ripple up counter using JK FFs.	**03**
	(b)	Write a brief note on quantization and encoding.	**04**
	(c)	List out various commonly used A/D converters. Draw & explain Flash A/D converter with necessary decoding table. Also mention pros & cons of the same.	**07**

****