Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(NEW) EXAMINATION – SUMMER 2023

Subject Code:3131102 Date:28-07-2023

Subject Name:Digital System Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Convert the following numbers form given base to the base indicates. (1) $(AEF2.B6)_{16}$ = (_____)$_2$ (2) $(674.12)_8$ = (_____)$_{10}$ (3) $(110110.1011)_2$ = (_____)$_{16}$	**03**
	(b)	Sate and prove DeMorgan's Theorem.	**04**
	(c)	simplify the following Boolean function, f(w,x,y,z)=∑m(2,6,8,9,10,11,14,15) using Quine-McClukey tabular Method.	**07**
Q.2	**(a)**	Obtain canonical Sum of Product form of following function: F=AB+ACD.	**03**
	(b)	Show that NAND & NOR are universal gates.	**04**
	(c)	Implement the following Boolean functions with a multiplexer and Decoder. F(w, x, y, z) = Σ (2, 3, 5, 6, 11, 14, 15)	**07**
		OR	
	(c)	Design and implement binary to gray code converter.	**07**
Q.3	**(a)**	Implement 8x1 MUX using 4x1 MUX.	**03**
	(b)	Give the comparison between synchronous and asynchronous counters.	**04**
	(c)	Explain JK flip flop with its characteristic table and excitation table.	**07**
		OR	
Q.3	**(a)**	What is race around condition in JK flip flop?	**03**
	(b)	Implement 4x16 decoder using two 3x8 decoder.	**04**
	(c)	Explain Master Slave JK flip-flop with truth table and circuit diagram	**07**
Q.4	**(a)**	Define following terms w.r.t Digital Logic Family: 1. Figure of merit 2.Noise Margin 3. Power Dissipation	**03**
	(b)	Describe General State Machine Architecture with suitable diagrams.	**04**
	(c)	Compare ROM, PLA and PAL.	**07**
		OR	
Q.4	**(a)**	Define following terms w.r.t State Machine 1. State Table 2. State Diagram	**03**
	(b)	Give classification of logic families. Also list the characteristics of digital IC.	**04**
	(c)	Explain Moore machine.	**07**
Q.5	**(a)**	List the steps in VLSI Design flow.	**03**
	(b)	Design Modulo-8 counter using T flip flop.	**04**

	(c)	With neat sketch design 4-bit bidirectional shift register.	**07**

OR

Q.5	**(a)**	Explain the problem associate of an asynchronous state machine with the help of one example.	**03**
	(b)	Design 3-bit synchronous up counter using T flip flop.	**04**
	(c)	Design 4-bit ripple counter using negative edge triggered JK flip flop.	**07**

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