Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–1 (NEW) EXAMINATION – WINTER 2018

Subject Code: 3710512 **Date: 03/01/2019**

Subject Name: RTL Simulation and Synthesis with PLDs

Time: 02:30 PM To 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full mark**

Q.1	**(a)**	Explain FPGA design flow.	**07**
	(b)	Explain metastability.	**07**
Q.2	**(a)**	Define setup time, hold time with respect to flip flop.	**07**
	(b)	Design a counter which counts sequence 1,2,4,6,0. Using D Flip Flop.	**07**
		OR	
	(b)	Explain the steps involved in physical verification.	**07**
Q.3	**(a)**	How a latch gets inferred in RTL design?	**07**
	(b)	Difference between PLDs and FPGA	**07**
		OR	
Q.3	**(a)**	Discuss design flow of floorplanning.	**07**
	(b)	Explain variable biasing technique	**07**
Q.4	**(a)**	Explain top down approach.	**07**
	(b)	What is skew, what are problems associated with it and how to minimize it?	**07**
		OR	
Q.4	**(a)**	Explain bottom up approach.	**07**
	(b)	Implement half subtractor using primitive gates structural in verilog.	**07**
Q.5	**(a)**	Explain different sources of power dissipation in digital CMOS circuit.	**07**
	(b)	What is glitches & Explain techniques to reduce glitches.	**07**
		OR	
Q.5	**(a)**	Design a FSM for detecting a sequence of 1010 overlapping sequence..	**07**
	(b)	Gray codes have the useful property that consecutive numbers differ in only a single bit position. Design a 3-bit Gray code counter FSM with no inputs and three outputs. When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching100, it should repeat from 000. Draw a schematic for this counter using T flip-flops.	**07**

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