Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER –I-(New) EXAMINATION – SUMMER 2019

Subject Code: 3710512 **Date: 10/05/2019**

Subject Name: RTL Simulation and Synthesis with PLDs

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What are Design Rule Check (DRC) and Layout Vs Schematic (LVS) ?.	**07**
	(b)	What is Clock distribution network ?	**07**
Q.2	**(a)**	Define setup time, hold time with respect to flip flop.	**07**
	(b)	Design a counter which counts sequence 1,2,4,6,0. Using D Flip Flop.	**07**
		OR	
	(b)	Design a counter which counts sequence 3,4,5,7,3. Using T Flip Flop.	**07**
Q.3	**(a)**	Discuss floor planning in brief.	**07**
	(b)	What Physical timing closure?	**07**
		OR	
Q.3	**(a)**	Explain different types of routing.	**07**
	(b)	What is the difference between FPGA and ASIC?	**07**
Q.4	**(a)**	Explain clock tree synthesis.	**07**
	(b)	Explain FPGA Structure.	**07**
		OR	
Q.4	**(a)**	Explain why low power design is essential.	**07**
	(b)	Explain difference between floor planning & placement.	**07**
Q.5	**(a)**	Explain sleep transistor technique.	**07**
	(b)	What are RTL, Gate, Metal and FIB fixes? What is a "sewing kits"?.	**07**
		OR	
Q.5	**(a)**	Design a FSM for detecting a sequence of 1010 overlapping sequence.	**07**
	(b)	Design a combination lock as shown in the drawing below. Assume the internally known combinationC3C2C1C0as shown. The state of the lock is indicated by the output locked. Once unlocked (locked=0) the lock should remain unlocked until the lock input is true. Once locked, the lock will remain locked until it has seen the initition sequence “000” followed by the correct combinationC3= 0, C2=1, C1= 1, C0= 0 on the input. Design the internal logic of this lock (using D flip-flops) and draw the circuit that implements it.	**07**

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