Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**ME – SEMESTER – I (New)– EXAMINATION – WINTER-2019**

**Subject Code: 3710512** **Date: 09-01-2020**

**Subject Name: RTL Simulation and Synthesis with PLDs**

**Time: 02:30 PM TO 05:00 PM** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | Explain ASIC design flow. | **07** |
| | **(b)** | Explain metastability. | **07** |
| **Q.2** | **(a)** | What is glitch? What causes it (explain with waveform)? How to overcome it? | **07** |
| | **(b)** | Design a counter which counts sequence 0,3,4,7,0. Using D Flip Flop. | **07** |
| | | **OR** | |
| | **(b)** | Design a counter which counts sequence 0,1,2,6,0. Using T Flip Flop. | **07** |
| **Q.3** | **(a)** | Discuss floor planning in brief. | **07** |
| | **(b)** | Difference between PLDs and FPGA | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Discuss placement in brief. | **07** |
| | **(b)** | Difference between PLA & PAL. | **07** |
| **Q.4** | **(a)** | Explain ESD protection. | **07** |
| | **(b)** | Explain clock tree synthesis. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Explain why low power design is essential. | **07** |
| | **(b)** | Explain DTCMOS technique. | **07** |
| **Q.5** | **(a)** | Explain different sources of power dissipation in digital CMOS circuit. | **07** |
| | **(b)** | Explain difference between combinational & Sequential design. | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | Design a FSM for detecting a sequence of 1011. | **07** |
| | **(b)** | Write the state table from the state bubble diagram. Fill in the table given below. Use the following state assignments: START=000, GOT0=001,GOT01=010, GOT011=011and GOT0110=100. All unused states should go to the START state and output z= 0.Assume you will build the circuit with J-K flip-flops. | **07** |

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