Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER – I (New)– EXAMINATION – WINTER-2019

Subject Code: 3710515 **Date: 03-01-2020**

Subject Name: DSP Architecture

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	(a)	Differentiate between Von Neumann and Harvard Architecture.	07
	(b)	Draw and explain the block diagram of DSP system.	07
Q.2	(a)	How DSP architecture is beneficial in implementation of convolution algorithm?	07
	(b)	Explain the concept of pipelining with reference to DSP architecture.	07
		OR	
	(b)	Differentiate between fixed point and floating point processors.	07
Q.3	(a)	Explain IEEE standard for floating point computation.	07
	(b)	Explain the concept of parallelism in DSP architecture.	07
		OR	
Q.3	(a)	List the main features of TMS320C2X DSP processors.	07
	(b)	Draw and explain the block diagram of event managers in TMS320C2X DSP processors.	07
Q.4	(a)	Explain central arithmetic and logic unit of TMS320C2X DSP processor.	07
	(b)	List the on chip peripherals of TMS320C54X DSP processor.	07
		OR	
Q.4	(a)	List the addressing modes of TMS320C5X processor and explain indirect addressing mode in detail.	07
	(b)	Explain the concept of VLIW architecture.	07
Q.5	(a)	Draw and explain the functional block diagram of TMS320C67X DSP processor.	07
	(b)	Explain the concept of barrel shifter with proper diagram.	07
		OR	
Q.5	(a)	With an example show how FPGA outperforms DSPs for the implementation of high speed filters.	07
	(b)	Draw and explain the block diagram of one complete application of DSP based system.	07

****

GTUQuestionPapers.com